IN THE SPECIFICATION

Please amend the specification as follows:

Replace the paragraph on page 4, between lines 4-7 of the specification with the following:

Now, another object of the present invention is realized by the electronic circuit arrangement ~~of claim 6. Such an arrangement~~ that facilitates a built-in self-test for the electronic circuit, because the further electronic circuit can operate as the test device for the electronic circuit, which obviates the need for expensive dedicated tester equipment.

Replace the paragraph on page 4, between lines 11-14 of the specification with the following:

Now, yet another object of the invention is realized by the method of ~~claim 8. Interconnect~~ interconnect testing ~~by means of this method provides~~ to provide better fault detection compared to the method disclosed in the aforementioned prior art, because more interconnect faults at the output side of the electronic circuit

are detectable.

Replace the paragraph spanning pages 6-7, between page 6, line 13, and page 7, line 8 of the specification with the following:

An appropriate test pattern for the test unit as depicted in Fig.1 can be a sequential pattern of all 0's, of a walking 1, of all 0's and of a walking 0. In Table I, the detectable output signals at I/O nodes 131-135 resulting from such a pattern for a combinatorial circuit 160 implementing an XOR gate and an XNOR gate respectively, are listed for a fault-free electronic circuit 100 as shown in Fig. 1.

pattern number	I/O nodes 121-124	I/O nodes 131-135 (XOR gate)	I/O nodes 131-135 (XNOR gate)
1	0000	01010	01011
2	1000	11011	11010
3	0100	00011	00010
4	0010	01111	01110
5	0001	01001	01000
6	1111	10100	10101
7	0111	00101	00100

8	1011	11101	11100
9	1101	10001	10000
10	1110	10111	10110

Electronic circuit 100 can be brought in the test mode by several known ways, which for instance have been disclosed in the aforementioned European patent application EP 9901802. Main unit 180 can be arranged to switch the electronic circuit 100 to a test mode upon receipt of a predefined bit pattern or a sequence of predefined bit patterns via at least some of the I/O nodes from the first selection of I/O nodes 120, or main unit ~~120~~ 180 can be coupled to a dedicated test control node not shown, for switching the electronic circuit 100 to a test mode upon receipt of a test mode select signal. As another option, the test control node not shown can be coupled directly to the first selection of I/O nodes 120 and the second selection of I/O nodes 130 for connecting the I/O nodes to the test unit responsive to the test mode select signal.